Title	Code
Testing of Digital Circuits	**POZ04WTS2ICE34**
Field: **Electronics and Telecommunications**	Year / Semester: **2 / spring**
Specialty: **Information and Communication Technologies**	Course: **elective**
Hours / week: Lectures: **2** Classes: **-** Laboratory: **1** Projects / seminars:	Number of credits: **3**

Lecturer: **Prof. Jerzy Tyszer**
tel. +48 (61) 665 38 14, fax: +48 (61) 665 3823
e-mail: tyszer@et.put.poznan.pl

Faculty: **Electronics & Telecommunications**
ul. Polanka 3, 60-965 Poznań, Poland
tel. +48 (61) 665 2293, fax: +48 (61) 665 2572
e-mail: office@et.put.poznan.pl

Status of the course in the study program:

Elective course for students of electronics and telecommunications,
Specialization: information and communication technologies

Objectives of the course:

This course provides a comprehensive coverage of state-of-the-art digital circuit testing techniques, including practices and automation tools for high-quality low-cost manufacturing test. It aims at providing a clear picture of fundamental concepts, effective problem-solving techniques, and appropriate exposure to modern technologies, design techniques, and applications in the area of design for test. The presentation consists of balanced coverage of relevant ideas progressing through all levels of design and abstraction starting with transistor failures, moving through the gate and register levels, and concluding with an introduction to high level synthesis for testability. Furthermore, it reviews the newest topics related to embedded test methodologies developed specifically to reduce test data volume, test time, and yield learning. All lectures are illustrated with various applications and case studies.

Course description:

The course is a representative sample of the following topics. (1) Economics of test: semiconductor technology trends, designs characteristics of complex integrated circuits (logic, embedded memories, on-chip clocks, analog and mixed signal components), quality requirements (dpm, escapes, test coverage), defect level, test quality and yield, productivity requirements (time to market, design cycle), limitations of ATE (test accuracy, volume, bandwidth, test application time), cost of ATE (pin electronics, pin count, test application time), requirements for high quality low cost manufacturing test. (2) Fault modeling: taxonomy of failures (single and multiple, structural and functional, permanent and temporal), stuck-at faults, delay and transition faults, faults in CMOS technology, fault equivalence and dominance, fault collapsing, IDDQ tests, inductive fault analysis. (3) Test pattern generation: test definition and test generation basics, exhaustive and pseudo-exhaustive testing, structural deterministic test generation (basic flow, fault excitation and propagation, multiple path sensitization), testable and untestable faults, fault masking and redundancy, D algebra and principle algorithms, examples of ATPG solutions (D algorithm, Fan, Podem, recursive learning, Fastscan), gate delay fault model, path delay fault model, at-speed tests, sequential test generation. (4) Fault simulation: parallel simulation, deductive fault simulation, parallel-pattern single-fault propagation, concurrent fault simulation, critical path tracing, statistical fault analysis. (5) Design for testability (DFT): controllability and observability, ad hoc techniques, scan-based designs, scan-based test application, launch and capture techniques, complex capture windows, test point insertion, clock gating, level-sensitive scan design, boundary scan, low power scan operations. (6) Built-in self-test (BIST): pseudo-random tests, random pattern testability, weighted pseudorandom test generation, BIST-able circuits, generators of pseudorandom test patterns, test response compaction, error models and aliasing, compaction schemes, compaction in presence of unknown states, deterministic BIST, BIST controller, arithmetic BIST. (7) Fault diagnosis: fault dictionary, fault diagnosis for combi-

national circuits, effect-cause analysis, compaction of test responses and diagnostic resolution, random and deterministic scan partitioning, fault diagnosis in RAMs and ROMs. (8) Test data compression: cost of test (volume of test data, tester memory, test time), embedded and non-embedded test, replication of stimuli, repetition of stimuli, static reseeding, dynamic reseeding, architecture of embedded deterministic test, compression efficiency, modularization for IP cores and SoC applications, low power test data compression, low pin count testing applications. (9) Memory test: fault models (stuck-ats, transitions, couplings, pattern-sensitive failures), march tests, non-march test schemes, transparent testing, memory BIST architectures (Serial, Parallel), self-repair solutions, programmable memory BIST controller, BIST-in place for multiple embedded memories, insertion of memory BIST at RTL with multiple embedded arrays, multiple background and address scrambling, linking memory BIST and logic BIST, design of wrappers for embedded memories.

Prerequisite:

Basic knowledge of microelectronics and digital circuits.

Teaching methods:

Lectures supported by multimedia presentations, tutorials and laboratory projects.

Assessment methods:

Tests and written exam.

Bibliography:

1. M. Abramovici, M.A. Breuer, A.D. Friedman, *Digital systems testing and testable design*, IEEE Press, New York 1995.
2. L.-T. Wang, C.-W. Wu, X. Wen, *VLSI test principles and architectures*, Elsevier, Amsterdam 2006.
3. H. Jha, S. Gupta, *Testing of digital systems*, Cambridge University Press, Cambridge 2003.
4. J. Rajski, J. Tyszer, *Arithmetic built-in self-test*, Prentice Hall, Upper Sadle River 1998.
5. M.L. Bushnell, V.D. Agrawal, *Essentials of electronic testing*, Kluwer Academic Publishers, Boston 2000.